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Ozone 6 serial number1. Field of the Invention The present invention relates to a semiconductor memory, and more particularly to a data line driving circuit to drive a data line in a semiconductor memory. 2. Description of the Related Art In general, a semiconductor memory (hereinafter, referred to as a 'memory') includes a memory cell array in which a plurality of memory cells are arranged in rows and columns, a row decoder for selecting a memory cell row, and a column decoder for selecting a memory cell column. The memory cell array has a plurality of word lines that are provided to be in common with

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respect to the rows, a plurality of data lines that are provided to be in common with respect to the columns, and a plurality of cell plates that divide a memory cell that is provided between each of the word lines and the data lines. For example, a memory cell array includes a plurality of word lines WL0 to WL15 and a plurality of data lines DL0 to DL3. Each of the data lines DL0 to DL3 is divided into a first half of data lines and a second half of data lines by data lines clampers. The first half of the data lines is coupled to a plurality of word lines, and the second half of the data lines is coupled to a dummy memory cell through a data line clamp, thereby dividing the data lines into a memory cell region and a

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dummy memory cell region. Conventionally, each of the data lines is divided into the first half and the second half by each data line clamp. Here, when the divided data lines are driven to transfer data, generally, a first voltage  $V_{cc}$  is provided to a source of a driving transistor in a data line clamp, and a second voltage  $V_{ss}$  is provided to a source of the driving transistor in a data line. FIG. 1 is a circuit diagram of a data line driving circuit in a conventional semiconductor memory, and FIG. 2 is a timing diagram of an example.

Referring to FIG. 1, the data line driving circuit in a conventional semiconductor memory includes first and second PMOS transistors that are provided to correspond to the data lines DL and DLD,

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respectively, and first and second NMOS transistors that are provided to correspond to the data lines DL and DLD, respectively. The data line driving circuit includes inverters INV1, INV2, INV3 and INV4 that receive a signal CNT\_CDR\_LD c6a93da74d

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